

WHAT IS CLAIMED IS:

1. An integrated circuit device comprising:
at least one functional module which outputs save
data in synchronism with a saving clock signal;

5 a power supply control unit which selects one of
the functional modules, and controls stop and
resumption of power supply to the selected functional
module;

a save data storage unit which stores save data
10 output from a functional module selected by the power
supply control unit; and

an error checking and correction unit which
performs error checking and correction for the save
data stored in the save data storage unit when the save
15 data is to be restored to the functional module in
synchronism with a restoration clock signal.

2. A device according to claim 1, wherein the
error checking and correction unit comprises:

an encoder which generates an error correction
20 code from the save data, and writes the error
correction code in the save data storage unit; and

a decoder which reads out the stored save data and
the corresponding error correction code from the save
data storage unit, and decodes the save data.

25 3. A device according to claim 1, wherein
the error checking and correction unit periodically
performs error checking and correction for the save

data stored in the save data storage unit.

4. A device according to claim 1, wherein
the save data storage unit stores a plurality of
copies of the save data, and

5 the error checking and correction unit performs
error checking and correction by a majority operation
using said plurality of copied data stored in the save
data storage unit.

10 5. A device according to claim 1, wherein the
save data storage unit is storage means for a built-in
self-test circuit.

6. A device according to claim 1, which further
comprises:

15 a compressor which compresses the save data stored
in the save data storage unit; and

an expander which expands the save data compressed
by the compressor when the save data is to be restored
to the functional module.

20 7. A device according to claim 1, wherein the
save data storage unit is a volatile memory.

8. An integrated circuit device comprising:

25 at least one functional module which has
a plurality of flip-flops forming a scan chain,
performs a saving operation by outputting data in
the flip-flops by a shift operation using scan chain
synchronized with a saving clock signal, and performs
a restoring operation by restoring, to the flip-flops,

the saved data by a shift operation using scan chain
synchronized with a restoration clock signal;

5 a power supply control unit which selects one of
the functional modules, and controls stop and
resumption of power supply to the selected functional
module;

10 a clock signal generator which generates a saving
clock signal and restoration clock signal for the
functional module selected by the power supply control
unit;

15 a scan controller which, in the saving operation
or restoring operation, sets the functional module
selected by the power supply control unit to a scan
test mode, and selects the saving clock signal or
restoration clock signal generated by the clock signal
generator as a clock signal to be supplied for the
shift operation using scan chain;

20 a save data storage unit which stores the save
data output from the functional module selected by
the power supply control unit by the shift operation
using scan chain synchronized with the saving clock
signal; and

25 an error checking and correction unit which
performs error checking and correction for the save
data stored in the save data storage unit when the save
data is to be restored to the flip-flops of the
functional module by the shift operation using scan

chain synchronized with the restoration clock signal.

9. A device according to claim 8, wherein the clock signal generator generates a clock signal for use in periodic error checking and correction performed in the save data storage unit.

10. A device according to claim 8, wherein the error checking and correction unit comprises:

an encoder which generates an error correction code from the save data, and writes the error correction code in the save data storage unit; and

a decoder which reads out the stored save data and the corresponding error correction code from the save data storage unit, and decodes the save data.

11. A device according to claim 8, wherein the error checking and correction unit periodically performs error checking and correction for the save data stored in the save data storage unit.

12. A device according to claim 8, wherein the save data storage unit stores a plurality of copies of the save data, and

the error checking and correction unit performs error checking and correction by a majority operation using said plurality of copied data stored in the save data storage unit.

13. A device according to claim 8, wherein the save data storage unit is storage means for a built-in self-test circuit.

14. A device according to claim 8, which further comprises:

a compressor which compresses the save data stored in the save data storage unit; and

5 an expander which expands the save data compressed by the compressor when the save data is to be restored to the functional module.

15. A device according to claim 8, wherein the save data storage unit is a volatile memory.